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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,388	08/16/2007	Mark Nadim Olivier De Clercq	NL04 0156 US1	8723
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NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131				
EXAMINER				
CHAL LONGBIT				
ART UNIT		PAPER NUMBER		
2431				
NOTIFICATION DATE		DELIVERY MODE		
10/22/2008		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

**Office Action Summary****Application No.**

10/590,388

**Applicant(s)**DE CLERCQ, MARK NADIM  
OLIVIER**Examiner**

LONGBIT CHAI

**Art Unit**

2431

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 August 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 August 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 8/23/2006
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. Applicant's claim for benefit of domestic priority under 35 U.S.C. 119(e) is acknowledged.

The application is filed on 8/16/2007 but has a foreign priority application filed on 2/24/2004.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 3, 6 and 8 – 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Laackmann et al. (U.S. Patent 2003/0132777).

As per claim 1 and 10, Laackmann teaches an electronic device for cryptographic processing, comprising:

at least two electronic circuits coupled via a connection means, wherein the connection means is arranged for transferring data signals between the two electronic circuits (Laackmann: Figure 1, Para [0002], Para [0005] and Para [0072]),

characterized by a monitoring circuit arranged to monitor a deviation in the capacitance of the connection means and to generate an alert signal if the deviation exceeds a

predetermined value (Laackmann: Figure 1, Para [0002], Para [0005], Para [0072] and Para [0046]: (a) the change of capacitance can be detected and reported as a result of intrusive attack and (b) in the case of the capacitive measurement method, however, the signal receiver must receive approximately identical signal values).

As per claim 2, Laackmann teaches the monitoring circuit is arranged to monitor the data signals transferred via the connection means and to compare a monitored signal with a reference signal (Laackmann: Para [0046]: in the case of the capacitive measurement method, however, the signal receiver must receive approximately identical signal values).

As per claim 3, Laackmann teaches the electronic circuits comprise a logical circuit and a storage element arranged to store data output by the logical circuit (Laackmann: Figure 1).

As per claim 6, Laackmann teaches the monitoring circuit is arranged to monitor a value of the capacitance of the connection means and to compare the monitored value with a reference value (Laackmann: Para [0046]: in the case of the capacitive measurement method, however, the signal receiver must receive approximately identical signal values).

As per claim 8, Laackmann teaches a dummy electronic circuit having at least a dummy connection means with a capacitance comparable to that of the connection means, and wherein the monitoring circuit is further arranged to determine the reference signal by monitoring the dummy connection means when transferring a data signal identical to that transferred via the connection means (Laackmann: Para [0047]: there are two measurements, namely, normal measurement method and capacitance measurement method, which are changed back and

forth for a predetermined time interval and a different measurement signal must, then, correspondingly be received at the signal receiver in the case of the normal measurement method – Thereby, the capacitance measurement method is qualified as a dummy electronic circuit measurement with respect to the normal measurement method).

As per claim 9, Laackmann teaches the electronic device is further arranged to use the alert signal to power down at least a part of the electronic device (Laackmann: Para [0004]: an interruption or a short circuit attack is detected by an evaluation circuit that, then, directs the integrated circuit into a secure state which is triggering of a reset or the erasure of the memory contents).

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Laackmann et al. (U.S. Patent 2003/0132777), in view of Benkley (U.S. Patent 2003/0035570).

As per claim 4, Laackmann does not disclose expressly the monitoring circuit is a propagation delay detection circuit.

Benkley teaches the monitoring circuit is a propagation delay detection circuit (Benkley: Para [0090] / Last Para: the capacitance change can be evaluated as a time delay, which is also

a well-known electric theory that capacitance time constant is related to the magnitude of the capacitance).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Benkley within the system of Laackmann because (a) Laackmann teaches providing a mechanism for protecting an integrated circuit against reverse engineering (e.g. probing) by using a capacitance measurement method (Laackmann: Para [0012]), and (b) Benkley teaches the capacitance change can be evaluated as a time delay, which is also a well-known electric theory that capacitance time constant is related to the magnitude of the capacitance (Benkley: Para [0090] / Last Para).

4. Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laackmann et al. (U.S. Patent 2003/0132777), in view of Rayane et al. ("A Digital BIST for Operational Amplifiers Embedded in Mixed-Signal Circuits" Proceedings of IEEE VLSI Test Symposium; 1999, pp. 304-310).

As per claim 5, Laackmann does not disclose expressly the monitoring circuit is a slew-rate deviation detection circuit.

Rayane teaches the monitoring circuit is a slew-rate deviation detection circuit (Rayane: Section 2.1).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Rayane within the system of Laackmann because (a) Laackmann teaches providing a mechanism for protecting an integrated circuit against reverse engineering (e.g. probing) by using a capacitance measurement method and transmitting a random or periodically changing signal sequence to the target (Laackmann: Para

[0012] and [0047]), and (b) Rayane teaches providing an efficient technique of testing integrated circuit such as ASICs by using a slew-rate deviation detection method in the time domain (Rayane: Section 1 & 2.1).

As per claim 7, Laackmann does not disclose expressly the reference signal is derived from a Monte-Carlo analysis performed on the electronic device.

Rayane teaches the reference signal is derived from a Monte-Carlo analysis performed on the electronic device (Rayane: Section 4.1).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Rayane within the system of Laackmann because (a) Laackmann teaches providing a mechanism for protecting an integrated circuit against reverse engineering (e.g. probing) by using a capacitance measurement method and transmitting a random or periodically changing signal sequence to the target (Laackmann: Para [0012] and [0047]), and (b) Rayane teaches providing a high accuracy technique of the test response analysis in order to computer the variation of measurements due to tolerances for integrated circuit such (Rayane: Section 1 & 4.1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONGBIT CHAI whose telephone number is (571)272-3788. The examiner can normally be reached on Monday-Friday 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y. Vu can be reached on 571-272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Longbit Chai/

Longbit Chai Ph.D  
Primary Examiner, Art Unit 2431  
10/14/2008